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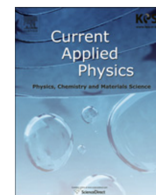

Suppression of bias stress-induced degradation of pentacene-TFT using MoO_x interlayer

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ABSTRACT

The bias stress effect in pentacene thin-film transistors (TFTs) with and without MoO_x interlayer was characterized. The device without MoO_x interlayer showed a large threshold voltage shift of 5.1 V after stressing with a constant gate-source voltage of −40 V for 10000 s, while at the same condition, the device with MoO_x interlayer showed a low threshold voltage shift of 1.9 V. The results can be attributed to the stable interface between MoO_x/pentacene and small contact resistance change for the device with MoO_x/Cu electrode. Pentacene-TFTs with MoO_x interlayer showed a high field-effect mobility of 0.61 cm^2/V s and excellent bias stability, which could be a significant step toward the commercialization of OTFT technology.

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1. Introduction

Pentacene-based thin film transistors (TFTs) have a strong potential to be used in emerging electronic devices including the thin film transistor backplanes for flexible displays or active matrix organic light-emitting diode (AM-OLED) displays because they offer high mobility, excellent uniformity [1–4]. To realize such applications, it is certainly necessary to obtain stable device characteristics under a various bias stress. Previous reports on pentacene-TFTs show that there are three distinct mechanisms responsible for the threshold voltage shift of pentacene-TFT, namely, defect generation analogous with a-Si TFTs, charge tunneling into gate insulator and charge trapping in the channel and contact region. Wang et al. [5] reported that both the contact and the channel have contribution to the BS instability in top-contact pentacene-TFTs. Most of works have showed that controlling the insulator surface is the most popular way for suppressing the bias stress-induced degradation [6–8]. Suemori et al. [9] have found that the relationship between the threshold voltage stability and the chemical species of the insulator surface by using pentacene field-effect transistors with different types of self-assembled monolayer on a SiO_2 insulator. Comparatively, less attention is paid to relation between the bias stress and contact resistance. Wang et al. [5] reported the observation in pentacene-TFTs that contact resistance is changing during the bias measurements, and the effect of the contact resistance change on the drain current decay can even exceed that of the channel resistance change arising from the threshold voltage shift.

MoO_x is lately drawing strong attention as a promising hole injection layer since it has a very high work function (5.6 eV) and high environmental stability [10,11]. MoO_x has been frequently used as HIL in organic light-emitting diodes (OLEDs) due to the significant enhancement in device efficiency and stability [12,13]. In previous work, we have reported that MoO_x interlayer can effectively reduce the contact resistance of pentacene-TFT [14]. Here, we examine the bias stability of pentacne-TFT with MoO_x interlayer and investigate the contact resistance change under bias stress for pentacene-TFT with and without MoO_x interlayer.

2. Experimental details

A cross section of the TC pentacene-based OTFTs is shown schematically in Fig. 1. The devices were fabricated using heavily-doped *p*-type silicon wafers with a 250-nm-thick SiO_2, which functioned as the gate electrode and the gate insulator, respectively. Prior to deposition, the wafers were cleaned with acetone, methanol, and de-ionized water in that order. Subsequently the wafer was treated with UV-ozone for 15 min. A 30 nm pentacene thin film as channel layer was then deposited by high vacuum deposition at a rate of ~0.05 nm/s under a pressure of 10^{-6} Torr.

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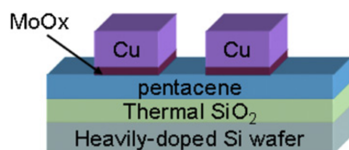

Fig. 1. Schematic cross section of pentacene-TFT with MoO_x/Cu source/drain electrode.

Then, the shadow mask was changed in a glove box ($O_2 < 1$ ppm, $H_2O < 1$ ppm), followed by transferring into a vacuum evaporation chamber without exposing to the air. An optimal thickness (4.0 nm) of MoO_x buffer layer and 60 nm Cu S-D electrodes were sequentially deposited onto pentacene layer using the same chamber. The MoO_x layer was deposited by thermal evaporation from MoO_3 powder at a pressure of 10^{-6} Torr (deposition rate: ~0.02 nm/s) and the Cu S-D electrodes were evaporated with a resistively heated tungsten boat. The channel width (W) was fixed at 1 mm and the channel lengths (L) were varied from 50 to 250 μm. For comparison, a control device with Cu-only electrodes was also fabricated.

The current–voltage characteristics of the devices were measured at the room temperature using an Agilent E3647A Dual output DC power supply and a Keithley 6485 Picoammeter. The thickness of film was monitored by using an oscillating quartz thickness monitor (SQC-222 Co-deposition Controller, Sigma Instruments). The capacitance measurements were conducted with an HP 4284A Precision LCR meter. An Atomic force microscope (AFM, nanonavi SPA-400 SPM) was used to investigate the surface properties of films. Conventional θ-2θ XRD studies on the pentacene films were carried out in Regaku (D/MAX 2500) diffractometer using CuKα radiation. All measurements were carried out at room temperature.

3. Results and discussion

Pentacene has very strong tendency to form crystalline structures. The electrical characteristics of pentacene film are influenced by the structure of the crystalline lattice. Fig. 2 shows the XRD pattern of the pentacene film used for the fabrication of pentacene-TFTs. The film exhibits four diffraction peaks corresponding to the (001′), (002′), (003′) and (004′) peaks. These diffraction peaks demonstrate the well-ordered property of pentacene film. The first order diffraction peak locates at 5.73°, which is identified as the "thin-film" phase. The crystal size of pentacene films was calculated using Scherrer's formula:$D = k\lambda/\beta\cos\theta$, where β is the full-width at half-maximum (FWHM) of XRD (001′) peak, k is a constant ($k = 0.89$), λ is wavelength of CuKα radiation, θ is the Bragg diffraction angle of the most intense (001′) peak. The crystal size for pentacene film is estimated to be 226.8 nm. Fig. 3 shows the surface morphology of the pentacene thin film by AFM. The root-mean-square (RMS) for surface roughness of the pentacene thin film is estimated to be 4.13 nm.

The bias stress effects of pentacene-TFTs without and with MoO_x interlayer at the applied gate bias of −40 V are investigated as a function of time, as shown in Fig. 4(a) and (b), respectively. The field-effect mobility was calculated at the saturation region from the following equation:

$$\mu = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \tag{1}$$

Where I_{DS} is the drain-source current, W is the width of channel, L is the length of channel ($L = 50$ μm), C_i is the capacitance per unit area of the insulator layer, V_{GS} is the gate voltage, μ is the saturation mobility and V_{th} is the threshold voltage. The field-effect mobility of fresh device with Cu-only electrode is estimated to be 0.13 cm^2/V s and threshold voltage is about −14.5 V. After stressing with a constant gate-source voltage of −40 V for 10000 s, the mobility and the threshold voltage are 0.05 cm^2/V s and −19.6 V, respectively. On the other hand, the fresh device with MoO_x/Cu electrode exhibited a higher mobility of 0.61 cm^2/V s and a lower threshold voltage is about −7.3 V. After 10000 s at the applied gate bias of −40 V, the mobility and the threshold voltage are 0.58 cm^2/V s and −9.2 V, respectively. Compared with the device with Cu-only electrode, the field-effect mobility and threshold voltage slowly degrade with bias time for the device with MoO_x/Cu electrode.

According to the above results, the normalized mobility (μ/μ_0) and the shift threshold voltage (ΔV_{th}) with stress time were shown in Fig. 5(a) and (b), respectively. The shift of the threshold voltage ΔV_{th} was 1.9 V for the device with MoO_x/Cu electrode and 5.1 V for the device with Cu-only electrode after 10000 s stress. It was found that the normalized mobility and ΔV_{th} of the device with Cu-only electrode were dramatically reduced with the stress time. However, for the device with MoO_x/Cu electrode, the field-effect mobility slowly degrades with stress time and only small shift of threshold voltage was observed. The results suggest that the bias stress stability of pentacene-TFT can be improved by inserting MoO_x thin film between the S/D electrode and pentacene layer. The results can be attributed to the stable interface between MoO_x/

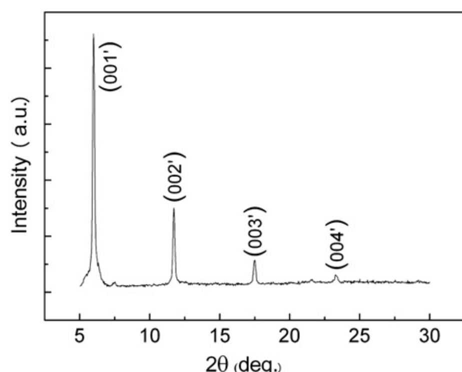

Fig. 2. XRD spectra of pentacene film grown on the thermally oxidized SiO_2 insulator.

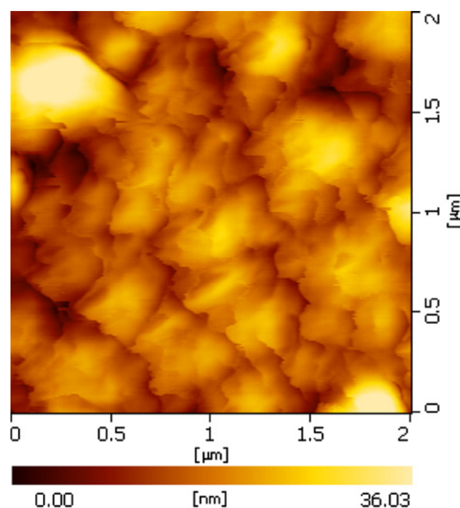

Fig. 3. surface morphology of the pentacene film grown on thermally oxidized SiO_2 insulator by AFM analysis.

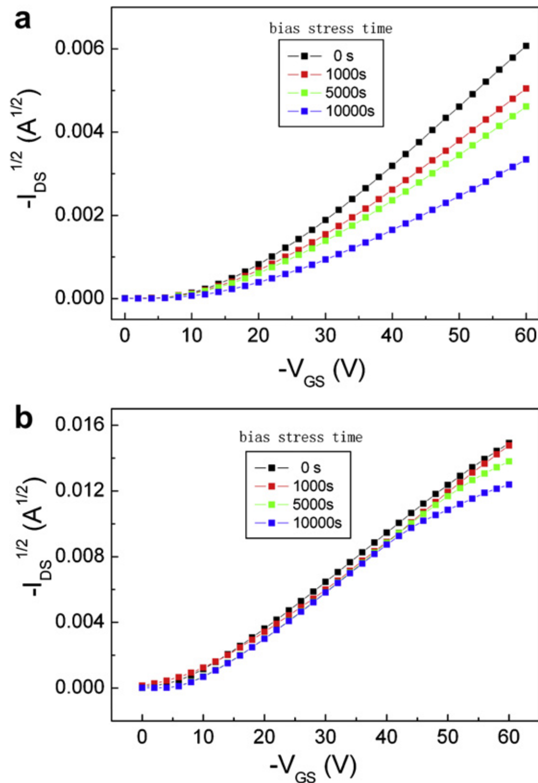

Fig. 4. Transfer characteristics before and after a bias voltage of −40 V for the two sets of TFTs: (a) Cu-only electrode; (b) MoO_x/Cu electrode.

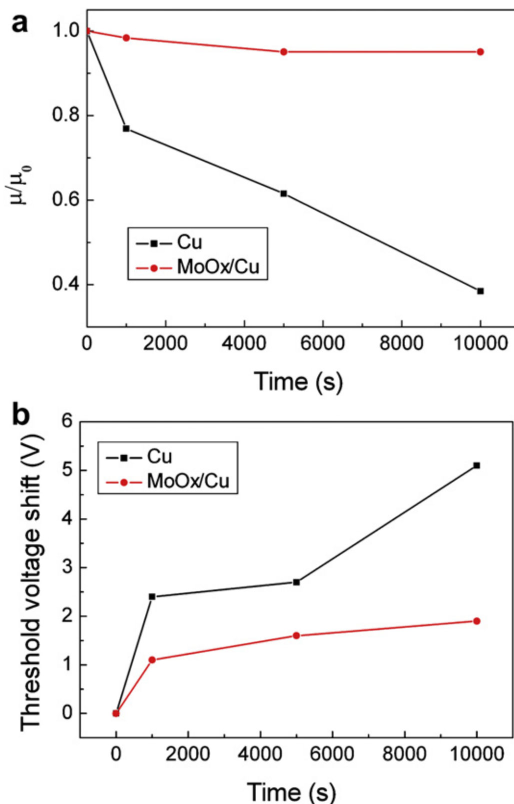

Fig. 5. (a) Normalized field-effect mobility (μ/μ_0) and (b) threshold voltage shift (ΔV_{th}) as a function of bias stress time.

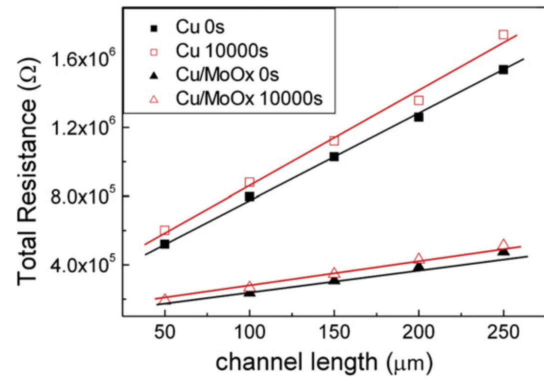

Fig. 6. shows the initial (t = 0 s) and final (t = 10000 s) transmission line method (TLM) plots under the bias stress voltage of −40 V for the two sets of TFTs (Cu and MoO_x/Cu).

pentacene and small contact resistance change for the device with MoO_x/Cu electrode.

In order to further analyze the contact resistance change, the transfer line method (TLM) was employed to calculate the contact resistance. Thus for small V_{DS} the measured resistance of the devices (R_{tot} defined as $\partial V_{DS}/\partial I_{DS}$) when modeled as the series combination of R_{ch}, R_S, R_D, is given by [15]

$$R_{tot} = R_{ch} + R_S + R_D \approx \frac{L}{W\mu_{ch}C_i(V_{GS} - V_T)} + R_C \quad (2)$$

Where $R_C = R_S + R_D$, μ_{ch} is the mobility of channel region. Equation (2) shows that the channel resistance is proportional to the channel length (L). More details were shown in the previous report [14]. Fig. 6 shows the initial (t = 0 s) and final (t = 10000 s) transmission line method (TLM) plots under the bias stress voltage of −40 V for the two sets of TFTs (Cu and MoO_x/Cu). The contact resistance of the device with and without MoO_x interlayer at a gate voltage of −40 V are 5.01 × 10^4Ω and 3.32 × 10^5Ω, respectively. However, after 10000 s bias stress, the contact resistance of the device with and without MoO_x interlayer at a gate voltage of −40 V are 5.26 × 10^4Ω and 4.5 × 10^5Ω, respectively. The contact resistance change for the device is shown in Fig. 7. During the bias stress measurements, I_{DS} in the line regime can be described as [5]:

$$I_{DS}(t) = \frac{V_{DS}}{\frac{L}{WC_iV_{GS} - V_{T0} - \Delta V_{th}(t)\mu_{ch}} + R_{C0} + \Delta R_C(t)} \quad (3)$$

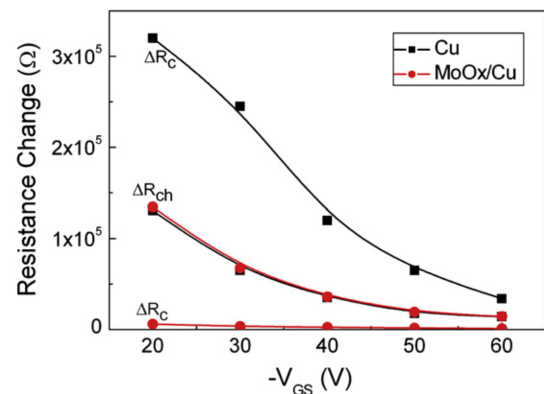

Fig. 7. Contact resistance change and channel resistance change (L = 50 μm) vs sweeping V_{GS} after 10000 s bias stress at stressing V_{GS} = −40 V.

Where V_{T0} and R_{C0} are the initial V_{th} and R_C, respectively. From the Eq.(3), it is easily seen that ΔV_{th} and ΔR_C are contributable to the bias stress effect. For the device with Cu-only, ΔR_C is much larger than ΔR_{Ch}, which will lead to the significant reduction of the field-effect mobility. In contrast, the MoO_x interlayer can supply more stable interface and show much smaller ΔR_C, so that only a little change of field-effect mobility was observed. In addition, pentacene-TFTs with MoO_x interlayer shows very similar channel properties (ΔR_{Ch}) with pentacene-TFTs without MoO_x interlayer. On the other hand, the contact instability may result from the charge trapping in the deep traps [5]. The larger ΔR_C for Cu-only contact suggest that there are much more deep traps at the Cu contact. In addition, the threshold voltage shift can be controlled according to the relationships [16]: $\Delta V_{th} = \Delta Q_{deep}/C_i$. By inserting MoO_x layer between Cu and pentacene film, more stable interface and less deep traps were achieved. Therefore, MoO_x interlayer is an effective way to suppress the bias stress-induced degradation of pentacene-TFTs.

4. Conclusions

In summary, we have suppressed the bias stress-induced instability of pentacene-TFTs using MoO_x interlayer between Cu and pentacene layer. Compared with pentacene-TFT without MoO_x interlayer, pentacene-TFT with MoO_x interlayer exhibited lower shift in field-effect mobility and threshold voltage after stressing with a constant gate-source voltage of −40 V for 10000 s. The results can be attributed to the stable interface between MoO_x/pentacene and small contact resistance change for the device with MoO_x/Cu electrode.

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References

[1] M. Mizukami, N. Hirohata, T. Iseki, K. Ohtawara, T. Tada, S. Yagyu, T. Abe, T. Suzuki, Y. Fujisaki, Y. Inoue, S. Tokito, T. Kurita, IEEE Electron Device Lett. 27 (2006) 249.
[2] S.C. Lim, S.H. Kim, H.Y. Chu, J.H. Lee, J. Lee, J.Y. Oh, D. Kim, T. Zyung, Synth. Met 151 (2005) 197.
[3] Christos D. Dimitrakopoulos, Patrick R.L. Malenfant, Adv. Mater. 14 (2002) 99.
[4] Robert A. Street, Adv. Mater. 21 (2009) 2007.
[5] S.D. Wang, T. Minari, T. Miyadera, Y. Aoyagi, K. Tsukagoshi, Appl. Phys. Lett. 92 (2008) 063305.
[6] U. Zschieschang, R.T. Weitz, K. Kern, H. Klauk, Appl. Phys. A 95 (2009) 139.
[7] Y.K. Moon, S. Lee, W.S. Kim, B.W. Kang, C.O. Jeong, D.H. Lee, J.W. Park, Appl. Phys. Lett. 95 (2009) 013507.
[8] T.N. Ng, J.H. Daniel, S. Sambandan, A.C. Arias, M.L. Chabinyc, R.A. Street, J. Appl. Phys. 103 (2008) 044506.
[9] K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, N. Takada, t. Kodzasa, T. Kamata, Appl. Phys. Lett. 91 (2007) 192112.
[10] D. Kumaki, T. Umeda, S. Tokito, Appl. Phys. Lett. 92 (2008) 013301.
[11] L. Cattin, F. Dahou, Y. Lare, M. Morsli, R. Tricot, S. Houari, A. Mokrani, K. Jondo, A. Khelil, K. Napo, J.C. Bernède, J. Appl. Phys. 105 (2009) 034507.
[12] Y. Yi, P.E. Jeon, H. Lee, K. Han, H.S. Kim, K. Jeong, S.W. Cho, J. Chem. Phys. 130 (2009) 094704.
[13] X.Y. Jiang, Z.L. Zhang, J. Cao, M.A. Khan, K. Haq, W.Q. Zhu, J. Phys. D: Appl. Phys. 40 (2007) 5553.
[14] J. Li, X.W. Zhang, L. Zhang, H. Zhang, X.Y. Jiang, X.Y. Jiang, K. Haq, W.Q. Zhu, Z.L. Zhang, Synth. Met 160 (2010) 376.
[15] J. Kanicki, F.R. Griffith, J. Griffith, R. Ploastre, J. Appl. Phys. 69 (1991) 2339.
[16] H. Kawaguchi, M. Taniguchi, T. Kawai, Appl. Phys. Lett. 94 (2009) 093305.